9VDC
> 500mA
REGULATED
J1
2x 1N4004
D8 D9
7.6 V
(USE HEATSINK)
IC13
7805
IN
OUT
GND
5 V
C3
10uF
35V
C4
10uF
35V

- OPTIONALLY ADD SEVERAL DECOUPLING CAPACITORS (0.1 uF) NEAR THE ICS.
- DIODES D8 & D9 ARE USED TO LOWER THE INPUT VOLTAGE TO IC13 (TO REDUCE HEATSINK TEMPERATURE), AND CAN BE OMMITTED IF NOT NEEDED.

14	22	22	14	16	40	14	1	1	14	1	14	14	1	14	1	14
V+	VCC	VCC	V+	VCC	VDD	V+	V+	V+	V+	V+	V+	VCC	VLED	VCC	VLED	V+
X2	IC1	IC2	IC3	IC4		IC5	IC6	IC7	IC8	IC9	IC10	IC11		IC12		IC14
ECS-100AC-010	2101 / 5101	2101 / 5101	4013	1802		4023	4050	4050	4016	4049	4016	TIL311		TIL311		4584 / 40106 / 74C14
GND	GND	GND	GND	VSS		GND	GND	GND	GND	GND	GND	GND		GND		GND
7	8	8	7	20		7	8	8	7	8	7	7		7		7

HIGH POWER CONSUMPTION PARTS SUCH AS IC11 & IC12 SHOULD HAVE THEIR POWER WIRING DIRECTLY TO IC13, INSTEAD OF DAISY-CHAINED WITH THE OTHER IC POWER WIRING.

IC3
4013
SET
CLK
D
RST
Q
$\overline{Q}$
NC

IC14
IC14
IC14
IC6
IC7

X2
1MHz
OSCILLATOR
ECS-100AC-010
1MHz
SLOW
50 ~ 1800 kHz
CW
X3
R12
1M
1.8 MHz CERAMIC RESONATOR

JUMPER, R12, X3, AND TWO SECTIONS OF IC14 ARE NOT REQUIRED IF ONLY THE 1MHz OSCILLATOR IS USED.

IC4
1802
CLOCK
XTAL
NC
A7 A6 A5 A4 A3 A2 A1 A0
D7 D6 D5 D4 D3 D2 D1 D0

FALLING EDGE OF 'CLEAR' INITIALIZES THE CPU.
RISING EDGE OF 'CLEAR' STARTS PROGRAM EXECUTION

SW4
RUN
UP
DN
IC7
$\overline{CLEAR}$

WITH SW1 ~ SW4, THE FOLLOWING BUFFER, OR PAIR OF INVERTERS, WITH OUTPUT TIED BACK TO INPUT, FUNCTIONS AS A SWITCH DEBOUNCE.

4x 47 k
R5 R6 R7 R8
$\overline{EF1}$ $\overline{EF2}$ $\overline{EF3}$ $\overline{EF4}$
I/O FLAGS

USE OF CMOS 5101 IS RECOMMENDED INSTEAD OF HIGHER POWER CONSUMPTION 2101.

IC1
2101 / 5101
256 x 4 STATIC RAM
IC2
2101 / 5101
256 x 4 STATIC RAM
A7 A6 A5 A4 A3 A2 A1 A0
CE2
$\overline{CE1}$
R / $\overline{W}$
OD
DO4 DI4 DO3 DI3 DO2 DI2 DO1 DI1

0 = MEMORY OUTPUTS ENABLED
1 = MEMORY OUTPUTS DISABLED
0 = WRITE ENABLE

SW1
IN
NO
NC
IC9
IC9
D1
1N914 / 1N4148
$\overline{IN}$

IC3
4013
SET
CLK
D
RST
Q
$\overline{Q}$
NC
D2
1N914 / 1N4148

PRESSING 'IN' ACTIVATES 'EF4' AND THIS CAN BE READ BY A RUNNING PROGRAM.
RELEASING 'IN' CLOCKS THE FLIP FLOP AND SETS ITS 'Q-NOT' LOW, PULLING 'DMA IN' LOW SO THE CPU WILL IMMEDIATELY READ THE SWITCHES AND WRITE THEIR DATA INTO THE CURRENT MEMORY LOCATION; WHEN THIS IS DONE, 'SC1' GOES HIGH AND RESETS THE FLIP FLOP.
THE FLIP FLOP IS NORMALLY HELD IN ITS RESET STATE EXCEPT WHEN IN 'LOAD' MODE.

3x 47 k
R2 R3 R4
$\overline{DMA\ IN}$
$\overline{DMA\ OUT}$
$\overline{INT}$

D3
1N914 / 1N4148
D4
1N914 / 1N4148
R9
47k
SC1
SC0
STATE CODE

$\overline{WAIT}$

SW2
LOAD
UP
DN
IC9
IC9
D5
1N914 / 1N4148
D6
1N914 / 1N4148
R10
47k
N2
N1
N0
N CODE
(I/O COMMANDS)

WHEN IN 'LOAD' MODE, THE LOGIC FOR STROBING IN THE SWITCH DATA AND STROBING OUT THE DISPLAY DATA IS ENABLED BY THE 'LOAD' SWITCH, VIA THE N2/LOAD SIGNAL. WHEN A PROGRAM IS RUNNING, THE 'N2' OUTPUT CAN BE CONTROLLED BY THE PROGRAM, AND THUS VIA THE N2/LOAD SIGNAL DATA MAY BE READ FROM SWITCHES AND WRITTEN TO THE DISPLAY.

R11
470
D7
'Q'
IC9
Q

TIMING
TPA
TPB
$\overline{MRD}$
$\overline{MWR}$

IC5
IC5
IC5
IC6
IC9
ALL INPUTS '1' TO STROBE DISPLAY
ALL INPUTS '1' TO STROBE SWITCHES
N2 / LOAD
STROBE DISPLAY
READ SWITCHES

J2
STEREO
AUDIO
OUTPUT
C5
10uF / 35V
IC14
R13
10k

J2, R13, C5, AND THIS SEGMENT OF IC14 ARE REQUIRED ONLY IF AUDIO OUTPUT IS DESIRED

SW3
MP
UP
DN
$\overline{WE}$
'WRITE ENABLE' ALLOWS MEMORY WRITES EXCEPT WHEN DISABLED BY THE 'MP' SWITCH BEING UP (ON)

IC8
4016
IC10
4016
X4B X3B X2B X1B
X4A X3A X2A X1A
C1 C2 C3 C4
SW5 - 7 -
SW6 - 6 -
SW7 - 5 -
SW8 - 4 -
SW9 - 3 -
SW10 - 2 -
SW11 - 1 -
SW12 - 0 -

IC11
IC12
D / 4
C / 2
B / 1
A / 0
BLANKING
R - DP
L - DP
$\overline{STB}$
TIL311
(LEFT / MSD)
(RIGHT / LSD)

THIS SCHEMATIC FAITHFULLY REPRODUCES THE ORIGINAL COSMAC 'ELF" COMPUTER CIRCUIT AS DESCRIBED IN THE AUGUST 1976 ISSUE OF POPULAR ELECTRONICS MAGAZINE.
- ADDITIONS: REPLACEMENT OF 1MHz CRYSTAL WITH HYBRID 1MHz OSCILLATOR, OPTION FOR SLOW RATE VARIABLE OSCILLATOR, OPTION FOR AUDIO OUTPUT.
- ALTERATIONS: REPLACEMENT OF ORIGINAL HP DISPLAY WITH TIL311 DISPLAY; APPEARANCE AND FUNCTION ARE IDENTICAL.
- NONE OF THE ENHANCEMENTS FROM SUBSEQUENT MAGAZINE ARTICLES ARE IMPLEMENTED IN THIS CIRCUIT.

CONTROL MODES

LOAD	RUN	
0	0	CLEAR / RESET
1	0	LOAD / REVIEW
0	1	RUN PROGRAM
1	1	WAIT / PAUSE

- '0' MEANS THAT 'LOAD' OR 'RUN' SWITCH(ES) ARE IN THEIR DOWN (OFF) POSITION.
- '1' MEANS THAT 'LOAD' OR 'RUN' SWITCH(ES) ARE IN THEIR UP (ON) POSITION.
- 'MP' SWITCH MUST BE IN ITS DOWN (OFF) POSITION WHEN LOADING A PROGRAM, AND IT MUST BE IN ITS UP (ON) POSITION WHEN REVIEWING A PROGRAM.

BASIC OPERATION:
1) 'LOAD', 'MP', 'RUN' ALL IN THEIR DOWN POSITIONS TO RESET PROGRAM COUNTER TO 0000.
2) RAISE 'LOAD' TO UP POSITION.
3) SET FIRST DATA BYTE ON TOGGLE SWITCHES, PRESS AND RELEASE 'IN' BUTTON.
4) THE DATA JUST ENTERED INTO MEMORY IS DISPLAYED.
5) PROGRAM COUNTER IS AUTOMATICALLY INCREMENTED.
6) REPEAT STEPS 3 - 5 FOR OTHER PROGRAM DATA BYTES.
7) WHEN PROGRAM HAS BEEN ENTERED, MOVE 'LOAD' TO DOWN POSITION, WHICH DISCONTINUES PROGRAM LOAD MODE AND ALSO RESETS PROGRAM COUNTER TO 0000.
8) RAISE 'MP' TO UP POSITION TO PREVENT MEMORY ALTERATION.
7) RAISE 'LOAD' SWITCH TO UP POSITION.
8) REPEATEDLY PRESS 'IN' BUTTON TO STEP THROUGH MEMORY, VIEWING PROGRAM DATA ON THE DISPLAY.
9) WHEN PROGRAM HAS BEEN REVIEWED AND VERIFIED, MOVE 'LOAD' SWITCH TO ITS DOWN POSITION.
10) MOVE 'RUN' SWITCH TO ITS UP POSITION TO RUN THE PROGRAM.
11) WITH THE PROGRAM RUNNING, RAISE THE 'LOAD' SWITCH TO TEMPORARILY PAUSE PROGRAM EXECUTION, LOWER THE 'LOAD' SWITCH TO RESUME PROGRAM EXECUTION.
11) MOVE 'RUN' SWITCH TO ITS DOWN POSITION TO STOP PROGRAM RXECUTION.

SHORT PROGRAM TO TEST THE "ELF"
(FLASHES THE 'Q' LED SLOWLY)

OP CODE	ADDRESS	MNE-MONIC	NAME
7A	0000	REQ	RESET 'Q' (= 0)
F8	0001	LDI	LOAD IMMEDIATE
10	0002		DATA = 10
B1	0003	PHI	PUT HIGH REG 1
21	0004	DEC	DECREMENT REG 1
91	0005	GHI	GET HIGH REG 1
3A	0006	BNZ	BRANCH IF 'D' NOT 0
04	0007		DATA = 04
31	0008	BQ	BRANCH IF 'Q' = 1
00	0009		DATA = 00
7B	000A	SEQ	SET 'Q' (= 1)
30	000B	BR	SHORT BRANCH
01	000C		DATA = 01

PROGRAM SETS 'Q' = 0 (OFF) THEN SETS THE HIGHER BYTE OF REGISTER 1 EQUAL TO 10 AND DOES A TIME DELAY BY REPEATEDLY DECREMENTING REGISTER 1 UNTIL ITS HIGHER BYTE = 00. THEN THE PROGRAM TOGGLES 'Q' TO THE OPPOSITE STATE AND REPEATS THE TIME DELAY, ETC.

COSMAC "ELF" SCHEMATIC DIAGRAM

DRAWN BY PAUL SCHMIDT ON MARCH 4, 2017