Preliminary CDP1831D, CDP1831CD

512-Word x 8-Bit Static Read-Only Memory

The RCA-CDP1831D and CDP1831CD are static 4096-bit mask-programmable COS/MOS read-only memories organized as 512 words x 8 bits and designed for use in CDP1800-series microprocessor systems. They will directly interface with either the CDP1801 or CDP1802 microprocessors without additional components.

The CDP1831 responds to 16-bit address multiplexed on 8 address lines. Address latches are provided on-chip to store the 8 most significant bits of the 16-bit address. By mask option, this ROM can be programmed to operate in any 512-word byte of 64K memory space. Three Chip-Select signals—CS1, CS2, $\overline{MRD}$—are also provided.

The polarity of the clock (TPA), and CS1 and CS2 are user mask-programmable. The Chip-Enable output signal (CEO) goes "high" when the device is selected. This signal is intended for use as an output disable control for small memory systems.

The CDP1831D is functionally identical to the CDP1831CD. The CDP1831D has a recommended operating voltage range of 3 to 12 volts, and the CDP1831CD has a recommended operating voltage range of 4 to 6 volts.

The CDP1831D and CDP1831CD are supplied in 24-lead, hermetic, dual-in-line ceramic packages.

Features:

- **Static Silicon-Gate CMOS circuitry—CD4000-series compatible**
- **Compatible with CDP1800-series microprocessors at maximum speed**
- **Interfaces with CDP1801, CDP1802 microprocessors without additional components**
- **Fast access time: 400 ns typ. at V_{DD} = 10 V**
- **Single voltage supply**
- **On-chip address latch**
- **Full military temperature range (−55°C to +125°C)**
- **Optional programmable location within 64K memory space**
- **Low quiescent and operating power**

MAXIMUM RATINGS,
Absolute-Maximum Values

Storage-Temperature Range (T_{stg}) ..... −65 to +150°C

Operating-Temperature Range (T_A) ..... −55 to +125°C

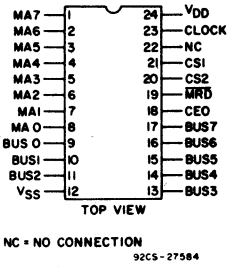
DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1831D ..... −0.5 to +15 V
CDP1831CD ..... −0.5 to +7 V

Power Dissipation Per Package (P_D):
For T_A=−55 to +100°C ..... 500 mW
For T_A=+100 to +125°C ..... Derate Linearly to 200 mW

Device Dissipation Per Output Transistor:
For T_A=−55°C to +125°C ..... 100 mW

Input Voltage Range, All Inputs ..... −0.5 to V_{DD} +0.5 V

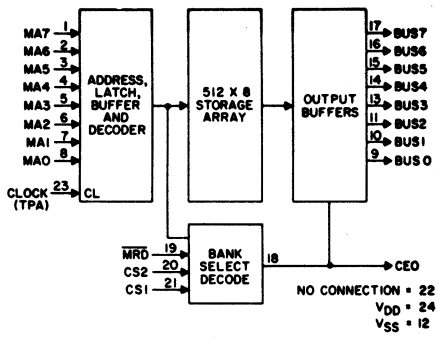
Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C



Terminal Assignment

OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS CDP1831D Min.	CDP1831D Max.	CDP1831CD Min.	CDP1831CD Max.	UNITS
Supply-Voltage Range (At T_A=Full Package-Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Clock Pulse Width (TPA), t_{PAW}		Typical		Typical		
	5	100		100		ns
	10	50		–		
Address Setup Time, t_{AS}	5	100		100		ns
	10	50		–		
Address Hold Time, t_{AH}	5	150		150		ns
	10	75		–		



CDP1832 Functional Diagram

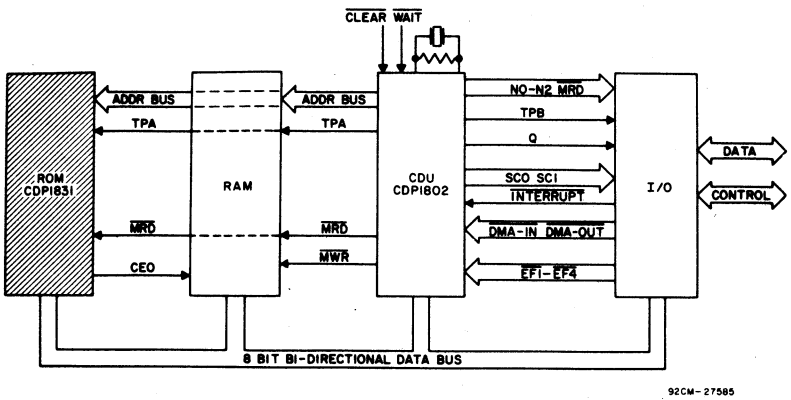
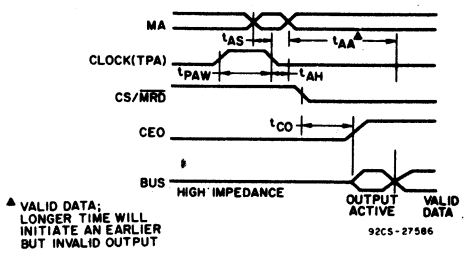


Fig. 1—Typical CDP1802 microprocessor system.



Timing Diagram

Preliminary CDP1831D, CDP1831CD

ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
			CDP1831D	CDP1831CD	
	V_O (V)	V_{DD} (V)	TYPICAL VALUES	TYPICAL VALUES	
Static					
Quiescent Device Current, I_L	–	5	100	100	μA
	–	10	500	–	
	–	15	1000	–	
Output Drive Current:					mA
N-Channel (Sink), I_DN	0.4	5	0.8	0.8	
	0.5	10	1.8	–	
P-Channel (Source), I_DP	4.6	5	–0.8	–0.8	
	9.5	10	–1.8	–	
Dynamic: t_r,t_f=10 ns, C_L=50 pF					
Access Time From Address Change, t_{AA}	–	5	850	850	ns
	–	10	400	–	
Chip Enable Output Delay Time From CS, t_{CO}	–	5	400	400	ns
	–	10	200	–	

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1831. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1831 is used with the CDP1802 microprocessor:

$t_{AH} = 0.5\ t_c$

$t_{PAW} = 1.0\ t_c$

$\overline{MRD}$ occurs one clock period (t_c) earlier than the address bits MA0-MA7.

where $t_c = \dfrac{1}{\text{CDP1802 clock frequency}}$

The CDP1831 is capable of operating at the maximum clock frequency of the CDP1802 microprocessor.