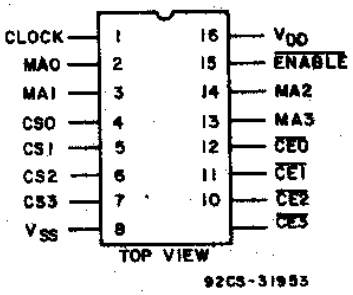
CDP1858, CDP1859 Types

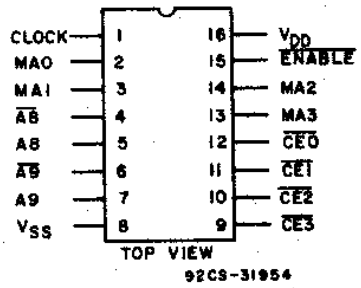
COS/MOS 4-Bit Latch With Decode

Features:

- **Static silicon-gate CMOS circuitry — CD4000-series compatible**
- **Provides easy connection of memory devices to CDP1802 microprocessor**
- **Single voltage supply**
- **Operating temperature range;**
  −55°C to +125°C (ceramic-package types)
  −40°C to +85°C (plastic-package types)
- **Low quiescent and operating power**
- **Non-inverting fully buffered data transfer**



CDP1858
TERMINAL ASSIGNMENT



CDP1859
TERMINAL ASSIGNMENT

RCA-CDP1858, CDP1858C, CDP1859, and CDP1859C are COS/MOS 4-bit latch decode circuits designed for use in CDP1800 series microprocessor systems. These devices have been specifically designed for use as memory-system decoders and interface directly with the CDP1802 or CDP1804 microprocessor multiplexed address bus at maximum clock frequency.

The CDP1858 and CDP1859 are functionally identical to the CDP1858C and CDP-1859C, respectively. The CDP1858 and CDP-1859 have a recommended operating-voltage range of 4 to 10.5 volts, and the CDP1858C and CDP1859C have a recommended operating-voltage range of 4 to 6.5 volts.

The CDP1858 interfaces the CDP1802 or CDP1804 address bus and up to 32 CDP-1822 256 x 4 RAM's to provide a 4K byte RAM system. No additional components are required. The CDP1858 generates the chip selects required by the CDP1822 RAM. The chip select outputs are a function of the address bits connected to inputs MA0 through MA3.

The MA0-MA3 address bits are latched at the trailing edge of TPA (generated by the CDP-1802). When $\overline{\text{ENABLE}}$=1 (V_{DD}), the CS outputs=0 (V_{SS}), and the CE outputs=1. When $\overline{\text{ENABLE}}$=0, the outputs are enabled and correspond to the binary decode of the inputs. The $\overline{\text{ENABLE}}$ input can be used for memory system expansion.

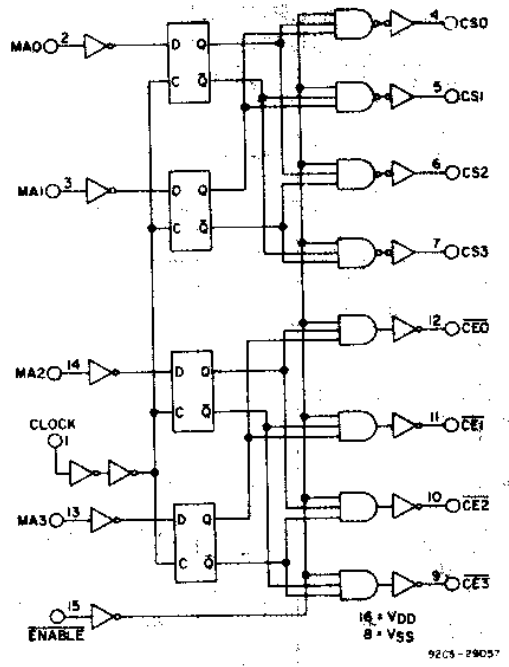
The CDP1858 is also compatible with non-multiplexed address bus microprocessors. By connecting the CLOCK input to 1 (V_{DD}), the latches are in the data following mode and the decoded outputs can be used in general-purpose memory-system applications.

The CDP1859 interfaces the CDP1802 or CDP1804 address bus and up to 32 CDP-1821 1024 x 1 RAM's to provide a 4K byte RAM system. The CDP1859 generates the chip selects required by the CDP1821 RAM. The chip select outputs are a function of the address bits connected to inputs MA2 and MA3. The address bits connected to inputs MA0 and MA1 are latched by the trailing edge of TPA (generated by the CDP1802 or CDP1804) to provide the two additional address lines required by the CDP1821 when used in a CDP1800 series microprocessor-based system. When $\overline{\text{ENABLE}}$=1, the CE outputs are 1's; when $\overline{\text{ENABLE}}$=0, and CE outputs are enabled and correspond to the binary decode of the MA2 and MA3 inputs. $\overline{\text{ENABLE}}$ does not affect the latching or state of outputs A8, $\overline{\text{A8}}$, A9, or $\overline{\text{A9}}$.

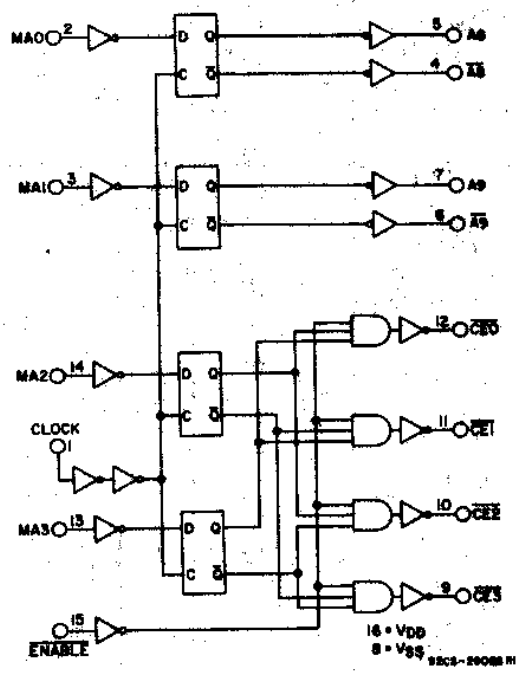
CDP 78 58

CDP1858, CDP1859 Types

The CDP1858, CDP1858C, CDP1859, and CDP1859C are supplied in 16-lead, hermetic, dual-in-line side-brazed ceramic packages (D suffix) and in 16-lead dual-in-line plastic packages (E suffix).



CDP1858 – Functional diagram.



CDP1859 – Functional diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal)
- **CDP1858, CDP1859** . . . . . −0.5 to +11 V
- **CDP1858C, CDP1859C** . . . . . −0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD}+0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
- For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
- For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . Derate Linearly at 12 mW/°C to 200 mW
- For T_A = −55 to +100°C (PACKAGE TYPE D) . . . . . 500 mW
- For T_A = +100 to +125°C (PACKAGE TYPE D) . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
- FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW

OPERATING-TEMPERATURE RANGE (T_A):
- PACKAGE TYPES D, H . . . . . −55 to +125°C
- PACKAGE TYPE E . . . . . −40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range.

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1858 CDP1859		CDP1858C CDP1859C		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

CDP1858, CDP1859 Types

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85°C$, Except as Noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1858 CDP1859			CDP1858C CDP1859C			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_L	—	0,5	5	—	0.1	10	—	5	50	μA
	—	0,10	10	—	1	100	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.6	3.2	—	1.6	3.2	—	mA
	0.5	0,10	10	2.6	5.2	—	—	—	—	
Output High Drive (Source Current), I_{OH}	4.6	0,5	5	−1.15	−2.3	—	−1.15	−2.3	—	mA
	9.5	0,10	10	−2.6	−5.2	—	—	—	—	
Output Voltage• Low-Level V_{OL}	—	0,5	5	—	0	0.1	—	0	0.1	V
	—	0,10	10	—	0	0.1	—	—	—	
Output Voltage• High-Level V_{OH}	—	0,5	5	4.9	5	—	4.9	5	—	
	—	0,10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	V
	0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	0.5,9.5	—	10	7	—	—	—	—	—	
Input Leakage Current, I_{IN}	Any Input	0,5	5	—	10^{-4}	±1	—	10^{-4}	±1	μA
		0,10	10	—	10^{-4}	±2	—	—	—	
Operating Current, I_{DD}▲	—	0,5	5	—	50	100	—	50	100	μA
	—	0,10	10	—	150	300	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	10	15	—	—	—	pF

*Tylcal values are for $T_A = 25°C$ and nominal voltage.

•$I_{OL} = I_{OH} = 1\ \mu A$.

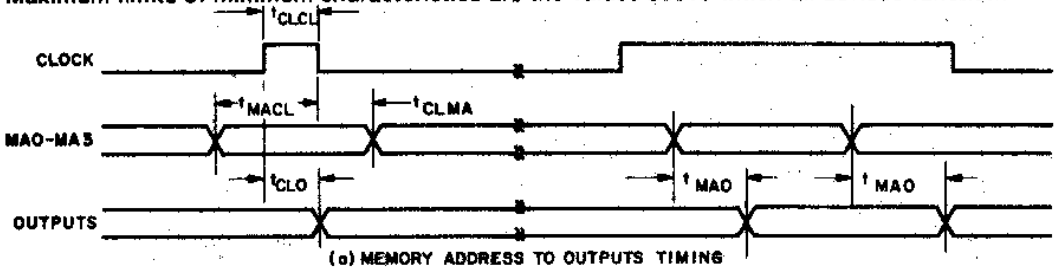
▲Measured in a CDP1802 or CDP1804 system at 2 MHz with open outputs.

CDP1858, CDP1859 Types

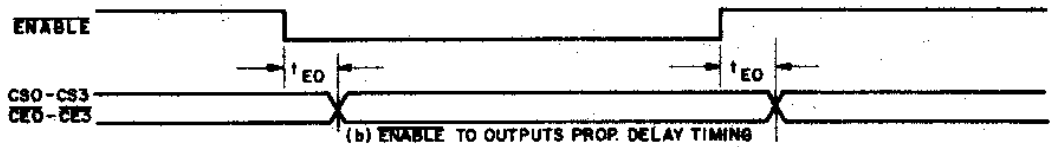
DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85$°C, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns, $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$, $C_L = 100$ pF, see Figs. 4 and 5.

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1858			CDP1858C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Minimum Setup Time, Memory Address to Clock, t_{MACL}	5	—	25	40	—	25	40	ns
	10	—	10	25	—	—	—	
Minimum Hold Time, Memory Address After Clock, t_{CLMA}	5	—	0	25	—	0	25	ns
	10	—	0	10	—	—	—	
Minimum Clock Pulse Width, t_{CLCL}	5	—	50	75	—	50	75	ns
	10	—	25	40	—	—	—	
Propagation Delay Times:								
Clock to Outputs, t_{CLO}	5	—	150	225	—	150	225	ns
	10	—	75	125	—	—	—	
Memory Address to Outputs, t_{MAO}	5	—	150	225	—	150	225	
	10	—	75	125	—	—	—	
$\overline{\text{ENABLE}}$ to Outputs, t_{EO}	5	—	125	200	—	125	200	
	10	—	65	100	—	—	—	
		CDP1859			CDP1859C			
Minimum Setup Time, Memory Address to Clock, t_{MACL}	5	—	25	40	—	25	40	ns
	10	—	10	25	—	—	—	
Minimum Hold Time, Memory Address After Clock, t_{CLMA}	5	—	0	25	—	0	25	ns
	10	—	0	10	—	—	—	
Minimum Clock Pulse Width, t_{CLCL}	5	—	50	75	—	50	75	ns
	10	—	25	40	—	—	—	
Propagation Delay Times:								
Clock to Address, t_{CLA}	5	—	125	200	—	125	200	ns
	10	—	65	100	—	—	—	
Clock to $\overline{\text{CHIP ENABLE}}$, t_{CLCE}	5	—	175	275	—	175	275	
	10	—	90	140	—	—	—	
Memory Address to Address, t_{MAA}	5	—	100	150	—	100	150	
	10	—	50	75	—	—	—	
Memory Address to $\overline{\text{CHIP ENABLE}}$, t_{MACE}	5	—	150	225	—	150	225	
	10	—	75	125	—	—	—	
$\overline{\text{ENABLE}}$ to $\overline{\text{CHIP ENABLE}}$, t_{ECE}	5	—	125	200	—	125	200	
	10	—	65	100	—	—	—	

Typical values are for $T_A = 25$°C and nominal voltages.
Maximum limits of minimum characteristics are the values above which all devices function.



(a) MEMORY ADDRESS TO OUTPUTS TIMING



(b) $\overline{\text{ENABLE}}$ TO OUTPUTS PROP. DELAY TIMING

Fig. 1 — CDP1858 timing diagram.

92CM-31956

CDP1858, CDP1859 Types

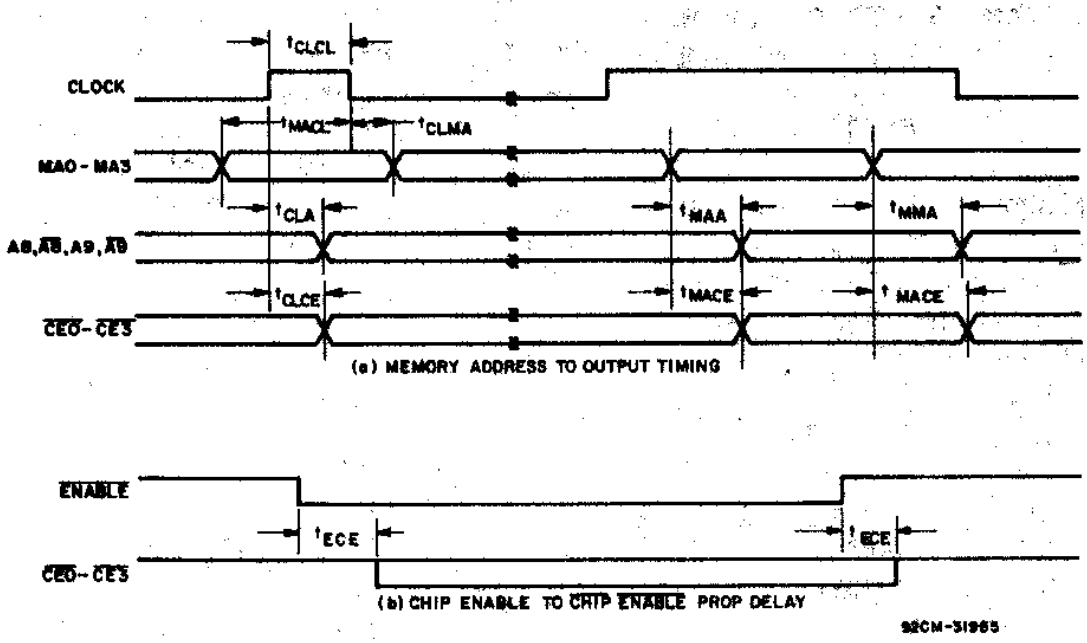


Fig. 2 – CDP1859 timing diagram.

CDP1858 DECODE TRUTH TABLE

$\overline{ENABLE}$	DATA INPUTS		CS0	CS1	CS2	CS3	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$
	MA1	MA0								
0	0	0	1	0	0	0	NOT AFFECTED BY MA1, MA0			
0	0	1	0	1	0	0				
0	1	0	0	0	1	0				
0	1	1	0	0	0	1				
	MA3	MA2								
0	0	0	NOT AFFECTED BY MA3, MA2				0	1	1	1
0	0	1					1	0	1	1
0	1	0					1	1	0	1
0	1	1					1	1	1	0
1	X	X	0	0	0	0	1	1	1	1

X = MA3, MA2, MA1, MA0 DON'T CARE

CDP1859 DECODE TRUTH TABLE

$\overline{ENABLE}$	DATA INPUTS		A8	A9	$\overline{A8}$	$\overline{A9}$	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$
	MA0	MA1								
0	0	0	0	0	1	1	NOT AFFECTED BY MA1, MA0			
0	0	1	0	1	1	0				
0	1	0	1	0	0	1				
0	1	1	1	1	0	0				
	MA3	MA2								
0	0	0	NOT AFFECTED BY MA3, MA2				0	1	1	1
0	0	1					1	0	1	1
0	1	0					1	1	0	1
0	1	1					1	1	1	0
1	X	X	NOT AFFECTED BY ENABLE				1	1	1	1

X = MA3, MA2, MA1, MA0 DON'T CARE