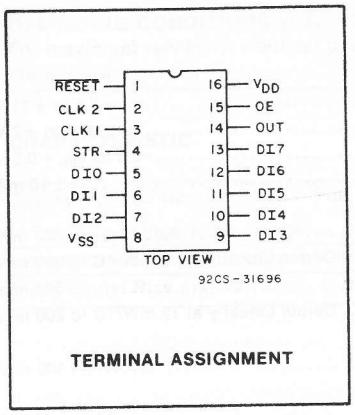

TERMINAL ASSIGNMENT

CMOS 8-Bit Programmable Frequency Generator

Features:

- *Directly interfaces with CDP1800-series microprocessors*
- *256 possible programmable frequencies*
- *Two clock input predividers (÷ 4 and ÷ 8)*
- *Gated square-wave output*
- *Single 4 to 10.5 V supply*

The RCA-CDP1863 and CDP1863C CMOS integrated circuits are programmable frequency generators designed to produce 256 possible frequencies from a single-frequency input clock. They will interface directly with the CDP1800-series microprocessor as shown in the system diagram (see Fig. 1).

The CDP1863 and CDP1863C consist of a programmable up-counter and an 8-bit latch (see Fig. 2). An input clock is predivided by a fixed internal counter chain in addition to the programmable counter. The final stage of the device divides the output of the up-counter by two to provide a square-wave output. The input clock may be applied to either of two inputs; CLK1 provides a divide-by-four predivide, and CLK2 a divide-by-eight. The unused input must be tied to V_{DD} to avoid interference with the true clock. After the programmable up-counter has reached its maximum count, the next predivided clock pulse will cause it to go to zero. At this time, the output flip-flop toggles and the load flip-flop is turned on. The output of the load flip-flop is fed into the NOR gates which allow the divide rate stored in the 8-bit latch to preset the up-counter. Before the next predivided clock pulse clocks this up-counter, the load flip-flop is reset and the NOR gates are turned off. The counter then resumes its up-count. The data at the eight data inputs is latched into the device by the high-to-low transition of CLK1, when STR(STROBE) is high, or by the high-to-low transition of STR, when CLK1 is high.

When using CLK2, CLK1 must be tied to V_{DD} to permit the STR input to generate the internal latch clock. The 8-bit data in the latch determines the divide rate of the programmable up-counter in the device. This rate may range from divide-by-one to divide-by-256.

A low level on the $\overline{\text{RESET}}$ input resets the up-counter, predividers, and flip-flops, and forces an initial state into the 8-bit data latch. This initial state provides a fixed divide rate for the device prior to running the system. A high level on the $\overline{\text{RESET}}$ input enables the up-counter, predividers, and flip-flops and allows programming a new divide rate into the device.

The CDP1863 and CDP1863C are functionally identical. They differ in that the CDP1863 has an operating voltage range of 4 to 10.5 volts and the CDP1863C has an operating voltage range of 4 to 6.5 volts. Both are supplied in 16-lead hermetic dual-in-line ceramic packages (D suffix) and in 16-lead dual-in-line plastic packages (E suffix).

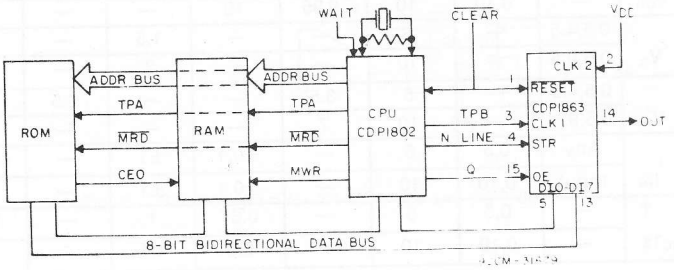

Fig. 1 — Typical CDP1800-series microprocessor system using the CDP1863 and CDP1863C.

CDP1863, CDP1863C

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(Voltage referenced to V_{SS} Terminal)
CDP1863 ..... −0.5 to +11 V
CDP1863C ..... −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D ..... −55 to +125°C
PACKAGE TYPE E ..... −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

STATIC ELECTRICAL CHARACTERISTICS *at T_A = −40 to +85°C, except as noted*

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1863			CDP1863C			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
Quiescent Device Current, I_L	—	—	5	—	50	250	—	50	250	μA
	—	—	10	—	250	500	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.6	2.2	—	1.6	2.2	—	mA
	0.4	0,10	10	3	3.6	—	—	—	—	
Output High Drive (Source) Current, I_{OH}	4.5	0,5	5	−1	−1.6	—	−1	−1.6	—	mA
	9.5	0,10	10	−3	−3.6	—	—	—	—	
Output Voltage Low-Level, V_{OL}	—	0,5	5	—	0	0.05	—	0	0.05	V
	—	0,10	10	—	0	0.05	—	—	—	
Output Voltage High-Level, V_{OH}	—	0,5	5	4.95	5	—	4.95	5		
	—	0,10	10	9.95	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	V
	0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	0.5,9.5	—	10	7	—	—	—	—	—	
Input Leakage Current, I_{IN}	Any	0,5	5	—	±0.1	±1	—	±0.1	±1	μA
	Input	0,10	10	—	±0.1	±1	—	—	—	
Operating Current † I_{DD}1‡	—	0,5	5	—	0.67	1	—	0.67	1	mA
	—	0,10	10	—	3.5	4.5	—	—	—	

*Typical values are for T_A = 25°C
†Measured with CLK1=2 MHz, total divide rate of 8, C_L = 50 pF.
‡Measured with CLK1=4 MHz, total divide rate of 8, C_L = 50 pF.

OPERATING CONDITIONS *at T_A = 25° C Unless Otherwise Specified*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

CHARACTERISTIC	LIMITS				UNITS
	CDP1863		CDP1863C		
	MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (At T_A = Full Package-Temperature Range)	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Input Signal Rise and Fall Time, t_r, t_f	—	· 5	—	5	μs

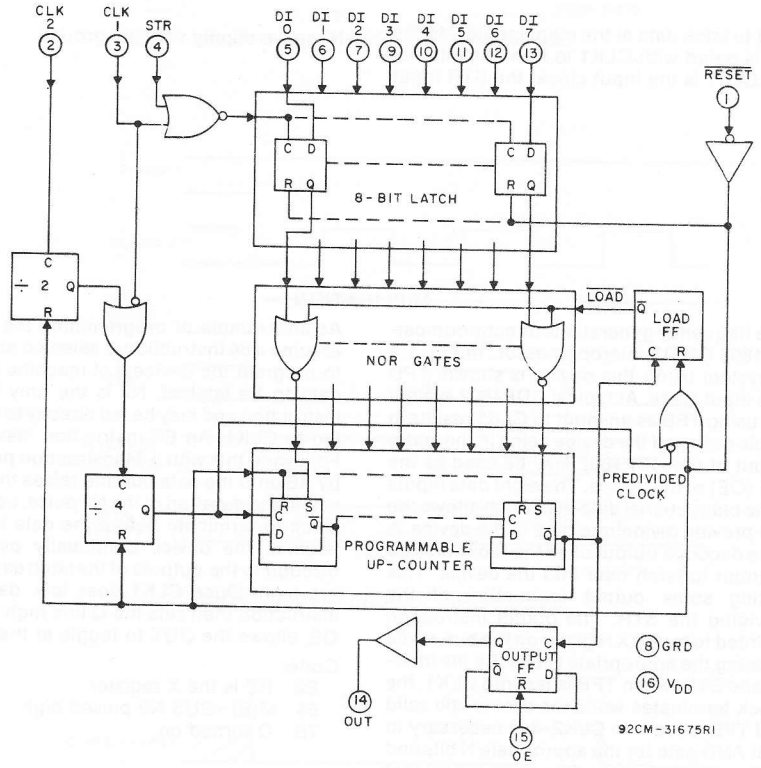

Fig. 2 — Block diagram for the CDP1863 and CDP1863C.

SIGNAL DESCRIPTIONS

CLK1, CLK2
Input clock which is divided-down by the device to provide an output frequency. The divide rate of the device is composed of a fixed predivide, the programmable divider, and a divide-by-two output flip-flop which provides a square-wave output. CLK1 is pre-divided by four and CLK2 is pre-divided by eight. The unused CLOCK input must be tied to V_{DD} to avoid interference with the true CLOCK signal. CLK1 may also be used to latch the eight data inputs.

OUT
Square-wave output which is the result of the divided-down input CLOCK. The OUTPUT toggles after the programmable up-counter reaches its maximum value and goes to zero. OUT is held low when OE is low.

OE
A high on this input allows OUT to toggle freely. A low on OE holds OUT low.

SIGNAL DESCRIPTIONS (Cont'd.)

D10-D17
Data inputs for programming the divide rate of the device. The divide rates programmed into the device are inversely proportional to the output frequencies generated. For example, programming the device with 00_{16} causes the programmable up-counter to divide by one, providing the maximum output frequency for any given input clock. Programming an FF_{16} results in the maximum divide rate and the minimum output frequency. To determine the frequency generated by a given programmed divide rate, divide the input clock frequency by the decimal equivalent of the programmed divide rate plus one, times the fixed predivide which is 8 for CLK1 or 16 or CLK2:

Input Clock Frequency/[(*Programmed Divide Rate* + 1)$_{10}$ (*Fixed Predivide*)]

STR
Positive pulse used to latch data at the eight inputs into the device. This pulse is gated with CLK1 to form the internal latch clock. When CLK1 is the input clock, the STR input must be positive during the high-to-low transition of CLK1. When CLK2 is the input clock, CLK1 must be tied to V_{DD} so that the STR input produces the latch clock.

$\overline{\text{RESET}}$
A low on the $\overline{\text{RESET}}$ input resets all the stages of the predividers and the programmable up-counter and sets an initial divide rate into the latch. This is to provide a standard initial divide rate at the moment the system begins running. A high on $\overline{\text{RESET}}$ enables the counter to run freely and allows programming a new divide rate. The initial state of the up-counter is a divide-by-54 resulting in a total divide rate of 432, after 1024 clock pulses when using CLK1, and 864, after 2048 clock pulses when using CLK2.

V_{DD}
Positive supply voltage.

V_{SS}
Negative supply voltage; ground.

APPLICATION

The programmable frequency generator is directly compatible with the CDP1802 CMOS microprocessor. In Fig. 1 a simple CDP1802 system using this device is shown. TPB may be used as the input clock. At typical CDP1802 system clock frequencies, using TPB as an input to CLK1 results in nearly every possible output of the device being in the audio range. The Q output of the CDP1802 may be used as the OUTPUT ENABLE (OE) of the device. The eight data inputs are connected to the bidirectional data bus which allows the system memory to provide divide rate data to the device. A single N bit or some decoded output of all the N bits may be used as the STR input to latch data into the device. This involves designating some output instruction of the CDP1802 for providing the STR. The output instruction places the data pointed to by the X register on the bus, while simultaneously pulsing the appropriate N bits. By the internal gating of TPB and STR, when TPB is fed into CLK1, the resulting latch clock terminates while the data is still valid on the 8-bit bus. If TPB is fed into CLK2, it is necessary to provide an external AND gate for the appropriate N bits and TPB, to preserve this timing feature. The same signal that feeds the $\overline{\text{CLEAR}}$ input of the CDP1802 may be used as the $\overline{\text{RESET}}$ signal to this device.

As an example of programming the frequency generator, assume a 64 instruction is selected as the output code used to program the device. Let machine register E point to the data to be latched. N2 is the only N bit pulsed by a 64 instruction and may be fed directly to the STR input if TPB is fed to CLK1. An EE instruction makes RE the X register. Following this with a 64 instruction puts the data pointed to by RE onto the data bus and raises the N2 bit. TPB, which is within the duration of the N2 pulse, causes the internal latch clock to terminate before the data bus loses validity. The latch in the device continually passes the data inputs through to the outputs of the latch as long as CLK1 and STR are high. Once CLK1 goes low, data is locked in. A 7B instruction then sets the Q line high which, if connected to OE, allows the OUT to toggle at the desired rate.

Code:

EE	RE is the X register
64	M(E)→BUS N2 pulsed high
7B	Q turned on

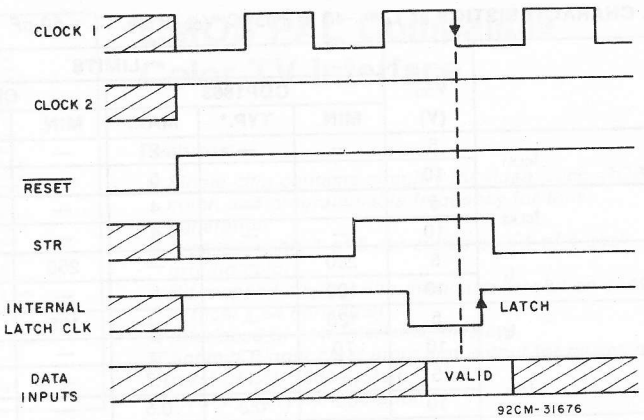

Fig. 3 — General CLOCK 1 timing diagram.

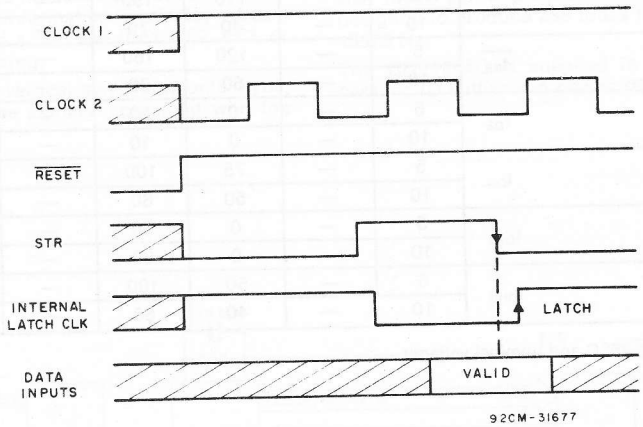

Fig. 4 — General CLOCK 2 timing diagram.

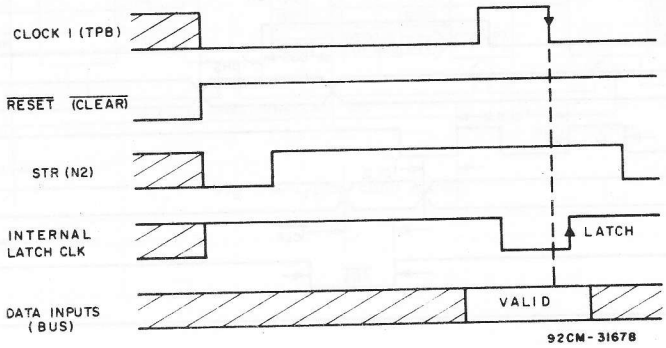

Fig. 5 — General CDP1800-series microprocessor system timing diagram.

CDP1863, CDP1863C

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = −40 to +85° C, V_{DD} ± 5%, C_L = 50 pF*

CHARACTERISTIC		V_{DD} (V)	LIMITS						UNITS
			CDP1863			CDP1863C			
			MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
Clock 1 Frequency	t_{CLK1}	5	—	—	2	—	—	2	MHz
		10	—	—	5	—	—	—	
Clock 2 Frequency	t_{CLK2}	5	—	—	4	—	—	4	MHz
		10	—	—	8	—	—	—	
Clock 1 Width	t_1	5	250	—	—	250	—	—	ns
		10	100	—	—	—	—	—	
Clock 2 Width	t_2	5	125	—	—	125	—	—	ns
		10	70	—	—	—	—	—	
Clock 1 to Clockout	t_{CL1}	5	—	1	1.7	—	1	1.7	μs
		10	—	0.3	0.5	—	—	—	
Clock 2 to Clockout	t_{CL2}	5	—	0.9	1.2	—	0.9	1.2	μs
		10	—	0.3	0.5	—	—	—	
$\overline{\text{Reset}}$ to Clockout	$t_{\overline{CLR}}$	5	—	260	375	—	260	375	ns
		10	—	130	170	—	—	—	
OE Delay to Clockout	t_{OED}	5	—	110	150	—	110	150	ns
		10	—	40	70	—	—	—	
$\overline{\text{Reset}}$ Pulse Width	$t_{\overline{RS}}$	5	—	120	160	—	120	160	ns
		10	—	60	90	—	—	—	
Data Setup to Clock 1	t_{DS}	5	—	0	20	—	0	20	ns
		10	—	0	10	—	—	—	
Data Hold to Clock 1	t_{DH}	5	—	75	100	—	75	100	ns
		10	—	50	80	—	—	—	
Data Setup to Strobe	t_{DSS}	5	—	0	30	—	0	30	ns
		10	—	0	30	—	—	—	
Data Hold to Strobe	t_{DHS}	5	—	50	100	—	50	100	ns
		10	—	40	60	—	—	—	

*Typical values are for T_A = 25° C and nominal voltages.

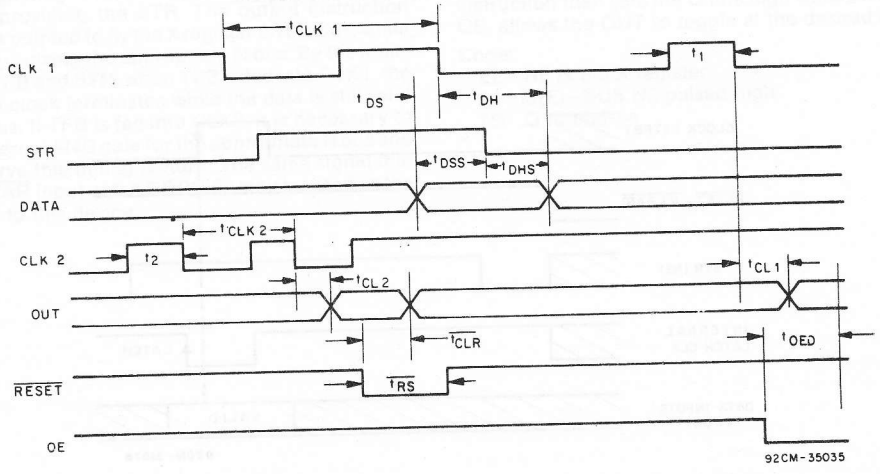

Fig. 6 — Timing diagram for the CDP1863 and CDP1863C.